09/735,944
Art Unit: 2634

In the claims

Please amend the claims as follows. This listing of the claims replaces all previous versions on file.

1.(currently amended) A multimode clock recovery circuit for use in the provision of constant bit rate services in a cell relay network, comprising:

a digital phase locked loop including a digital controlled oscillator for generating an output signal, a loop filter responsive to a phase signal to control said digital controlled oscillator, and a phase detector having multiple inputs for receiving different types of input signal;

said phase detector comparing an input signal applied to any of said multiple inputs with said output signal to develop said phase signal;

a local Synchronous Residual Timestamp Generator~~SRTS~~ generator for generating time stamps from said output signal connected to one of said multiple inputs of said phase detector;

said phase detector in SRTS mode developing said phase signal from said locally generated time stamps and time stamps received over said cell relay network;

another of said multiple inputs of said phase detector being adapted to receive a line rate clock signal;

said phase detector in a line rate mode developing said phase signal from said line rate clock signal and said output signal; and

a receive buffer for receiving incoming cells that in an adaptive mode develops said phase signal from a state of said buffer and applies said phase signal developed by said receive buffer to said loop filter to control said digital controlled oscillator.

2.(currently amended) A multimode clock recovery circuit as claimed in claim 1, wherein said receive buffer develops said phase signal in the form of a phaseword based on ~~the~~ a fill level thereof.

3.(previously presented) A multimode clock recovery circuit as claimed in claim 2, wherein said phaseword is derived from the write_pointer – read_pointer – *average* of said receive buffer, where *average* is a parameter set by the user.

4.(cancelled)

5.(currently amended) A multimode clock recovery circuit as claimed in claim 1, wherein said phase detector comprises a common up/down counter for developing said phase signal in said SRTS mode ~~and~~ and said line rate modes.

6.(previously presented) A multimode clock recovery circuit as claimed in claim 5, wherein an output of said common up/down counter is fed to an accumulator.

7.(previously presented) A multimode clock recovery circuit as claimed in claim 6, comprising a shifter for adjusting the weight of the output of said common up/down counter.

8.(currently amended) A multimode clock recovery circuit as claimed in claim 7, wherein said shifter adjusts the weight of said common up/down counter according to whether said recovery circuit is in said SRTS mode or said line rate mode.

9.(currently amended) A multimode clock recovery circuit as claimed in claim 8, wherein said shifter sets the weight of said common up/down counter to sixteen for a timestamp signal and one for a clock signal.

10.(previously presented) A multimode clock recovery circuit as claimed in claim 1, wherein said phase detector comprises first and second difference circuits, each receiving at first and second inputs thereof current time stamps and delayed time stamps, said first difference circuit receiving time stamps from said cell relay network and said second difference circuit receiving time stamps generated by said local SRTS generator, said first and second difference circuits providing respective inputs to an up/down counter, a subtractor having inputs for respectively receiving time stamps received over said cell relay network and time stamps generated by said local SRTS generator, and an accumulator for receiving the outputs of said subtractor and said up/down counter to develop said phase signal.

11.(previously presented) A multimode clock recovery circuit as claimed in claim 10, wherein the output of said up/down counter is weighted.

12.(original) A multimode clock recovery circuit as claimed in claim 1, wherein said local SRTS generator comprises a divider for receiving a feedback signal from the output of the phase locked loop, a counter for receiving a network clock signal, and a register for generating local SRTS time stamps.

13.(currently amended) A multimode clock recovery circuit as claimed in claim 11, wherein said up/down counter is a non wrap around counter.

14.(currently amended) A multimode clock recovery circuit as claimed in claim 1, wherein the phase locked loop goes into a holdover mold wherein the output of the phase locked loop remains constant when a valid input signal is lost so as to maintain a constant frequency based on the last valid input signal.

15.(currently amended) A multimode clock recovery circuit as claimed in claim 1, wherein the phase locked loop goes into a holdover mode when any of the following conditions occur: the receiver buffer runs out of SRTS values in the SRTS mode, a virtual circuit through said network times out, and loss of synchronization is asserted in ~~a~~ the line rate mode.

16.(cancelled)

17.(cancelled)

18.(currently amended) A multimode clock recovery circuit for use in providing constant bit rate services in a cell relay network, comprising a phase detector having multiple inputs, a loop filter receiving the output of said phase detector, a digital controlled oscillator receiving the output of said loop filter, a jitter reduction circuit receiving the output of said digital controlled oscillator, a divider receiving the output of said jitter reduction circuit, and a local SRTS generator in a feedback loop connected to one of said multiple inputs of said phase detector, said local SRTS generator generating local time stamps derived from the output of said digital controlled oscillator, and said phase detector developing a phase signal for controlling said digital controlled oscillator from said local time stamps and time stamps received from said cell relay network, and wherein said local SRTS generator includes a wrap-around counter, said phase signal is developed from the difference between the time stamps received from said local SRTS generator and said time stamps received over said cell relay network, and said phase detector includes a weighted non-wrap around up/down counter having an output that is added to said difference.

19.(currently amended) A phase detector for recovering clock signals from received time stamps in a cell relay network providing constant bit rate services, comprising a first input for receiving a remote time stamp signal, a second input for receiving a locally generated time stamp

signal, comparators for comparing the current time stamps of said first input and said second input with the previous time stamps of said first input and second input to generate, a weighted non-wrap around up/down counter receiving the outputs of said respective comparators, a subtractor for deriving the difference between said remote time stamp and said locally generated time stamp, and an accumulator for adding the output of said subtractor to the output of said weighted non-wrap around up/down counter to generate a phase output signal for controlling a digital controlled oscillator.

20.(previously presented) A phase detector as claimed in claim 19 having an error input for receiving an error flag.

21.(previously presented) A phase detector as claimed in claim 19, further comprising a register connected to the output of said accumulator for temporarily storing the phase output.

22.(cancelled)

23.(cancelled)

24.(cancelled)